Coding Assisted Adaptive Thresholding for Sneak-Path Mitigation in Resistive Memories

Zehui Chen, Clayton Schoeny, and Lara Dolecek
Department of Electrical and Computer Engineering - University of California, Los Angeles

***Abstract*—In crossbar resistive memory, in which a memristor is positioned on each row-column intersection, the sneak-path problem is one of the main challenges for reliable readout. The sneak-path event can be described combinatorially and its adverse effect can be modeled as a parallel interference. In this paper, based on a high-rate coding scheme, we characterize the inter-cell dependency of sneak-path events probabilistically. Utilizing this dependency, we propose adaptive thresholding schemes for resistive memory readout using side information provided by precoded bits. This estimation theoretic approach effectively reduces the bit-error rate while maintaining low redundancy overhead and low complexity.**

I. Introduction

Crossbar resistive memory, in which a memristor is positioned on each row-column intersection of the crossbar structure, is considered to be a promising candidate to be used as a non-volatile memory device because of its many unique advantages including a simple structure and high density [1]. One fundamental problem in resistive memory that demands great attention from the research community is the *sneak-path* problem [2]. When a cell in a crossbar array is read, a voltage is applied on the memristor and the resistance is measured to determine whether it is in Low-Resistance State (logic 1) or High-Resistance State (logic 0). Sneak paths are undesirable paths in parallel of the selected cell traversing through unselected cells; the current going through the sneak paths makes the read operation unreliable. This problem is especially severe when a cell in High-Resistance State (logic 0) is read because parallel low resistances, due to sneak-paths, lower the resistance measured from the cell at High-Resistance State, thus causing difficulties in distinguishing between the Low-Resistance State and the High-Resistance State. Numerous works, at various system levels, propose treatments devoted to addressing the sneak-path problem. Different memory architectures, including modification of the cell and/or array structure, have been proposed to alleviate or eliminate the sneak-path problem [3], [4], [5], [6]. Circuit level approaches including grounding unselected cells and multi-stage reading have also been proposed [7], [4]. Progress in cell material that incorporates nonlinearities has also shown ability to alleviate the sneak-path problem [8]. The application of noise estimation is studied in [9]. Finally, information theoretic studies of sneak-path free arrays with coding solutions are carried out in [10], [11], [12].

Despite these intensive research efforts over the past few years, the sneak-path issue remains an open problem for future memory architecture designers. In [11], the sneak-path problem is formulated as an *estimation problem* in communication, and the effect of the sneak-path event is viewed as a *parallel interference*. The dependency of the sneak-path problem between two cells on the same row/column is studied in [10]. Based on these two previous works, we propose adaptive thresholding schemes dependent on side-information gathered through precoded bits, utilizing a high-rate coding construction and our probabilistic characterization of inter-cell dependency. This is the first work that exploits the inter-cell dependency in resistive memory to improve estimation accuracy, i.e., to mitigate the adverse effect of sneak-path problem. Simulation results show an order of magnitude improvement in terms of bit-error rate can be achieved.

The content of this paper is organized as follows. Section II provides modeling of the sneak-path event and its adverse effect. The coding construction used in this paper is also introduced in Section II. Section III formally characterizes the dependency between the precoded bits and the information bits by calculating their joint probabilities of the sneak-path event. In Section IV, the adaptive thresholding idea is introduced and the optimal thresholds for different cases are derived. Section V provides simulation results comparing our proposed scheme with the naive formulation. We conclude and discuss future research in Section VI.

II. Sneak path Modeling and the Diagonal-0 Coding

A. Sneak path Modeling

In this paper, as an initial step, we use the sneak-path definition in [10] with modification, and also restrict ourselves to a sneak-path of length 3. Other factor that affects the occurrence of sneak-path, such as wire resistance, is not considered in this paper and is left for future work. *Cell selectors* are widely used hardware to mitigate the problem of sneak-path. To each memristor cell, a selector device is added in series in order to prevent reverse current flowing in sneak paths [11]. Our model assumes cell selectors fail i.i.d. with probability p_f [11]. Let $A \in \{0,1\}^{n\times n}$ denote the data matrix representing data stored in a crossbar resistive memory of size $n \times n$, and let A_{ij} denote the bit value at cell (i,j). By our definition, a sneak-path event occurs at cell (i,j) if the following three conditions are met:

1) The bit value stored is 0.
2) There exists at least one combination of $c_1, r_1 \in [1,\cdots,n], c_1 \neq j, r_1 \neq i$ that induces a sneak-path defined by
$$A_{ic_1} = A_{r_1c_1} = A_{r_1j} = 1. \tag{1}$$
3) The selector at cell location (r_1, c_1) fails.

We define e_{ij} to be a boolean random variable denoting the occurrence of the sneak-path event at location (i, j), conditioned on the bit value stored at (i, j) being 0. That is, $e_{ij} = 1$ if and only if the cell stores a 0 and (i, j) incurs a sneak-path event. We also refer to e_{ij} as the sneak-path state of cell (i, j). Note that the sneak-path event is defined only for those cells that store 0s because the adverse effect of a sneak-path event on a cell that stores 1 is not detrimental to the read process.

Our modeling of the adverse effect of a sneak-path event is adapted from [11], and this adverse effect is modeled as a parallel interference as follows. We first define the 0 state resistance of memristor to be R_0 and the 1 state resistance of memristor to be R_1. We then denote r_{ij} to be the measured resistance value of cell (i, j) through some sensing circuit with a measurement noise η. Throughout this paper, η is assumed to be Gaussian with variance σ^2 [11]. The adverse effect of a sneak-path event is modeled as a parasitic resistor with value R_s that is parallel to the read cell. Together, we have the following model:

$$r_{ij} = \begin{cases} \left(\frac{1}{R_0} + \frac{e_{ij}}{R_s}\right)^{-1} + \eta & \text{when 0 is stored,} \\ R_1 + \eta & \text{when 1 is stored.} \end{cases} \quad (2)$$

In this paper, we assume $R_1 < (1/R_0 + 1/R_s)^{-1}$ to prevent degenerate scenarios in the following sections (in practice, this is a safe assumption).

B. The Diagonal-0 coding

In crossbar resistive memory, as noted in [10], it is not hard to observe that the occurrence of a sneak-path event at one cell is *not* independent of the occurrence of a sneak-path event at another cell. For example, knowing that $e_{ij} = 1$ increase the probability of $e_{ij'} = 1, j' \in [1, \cdots, n], j' \neq j$, as well as $e_{i'j} = 1, i' \in [1, \cdots, n], i' \neq i$. This special behavior of resistive memory presents natural difficulty to coding solutions when viewing the sneak-path event as a bit error. However, when viewing the effect of sneak-path event as a parallel interference, one can utilize this inter-cell dependency to develop better estimation schemes based on side information provided by cells with known bit values.

We note that two cells are correlated the most when they are on the same row or column. It is also observed in [2] that the location of the cell (i and j) does not affect the probability of e_{ij}. More specifically, in this context, knowledge of a sneak-path occurrence at a cell provides the same information for all other cells on the same row(column). We then propose the following coding construction to better utilize this inter-cell dependency.

Construction 1. *We defined A to be "diagonal-0" coded if A satisfy the following:*

$$A_{ii} = 0, \forall i \in \{1, ..., n\}.$$

An example of a *diagonal-0* coded array is shown in Figure 1 where X denotes an arbitrary information bit. With this simple coding construction, each cell at location (i, j), with $(i \neq j)$, has a cell that stores a 0 in its row and a cell that stores a 0 in its column; we will use this knowledge for our improved estimation schemes. In this work, we restrict the resistive memory array to be square for simplicity. Note that this construction has a code rate $(n-1)/n$ which goes to 1 asymptotically.

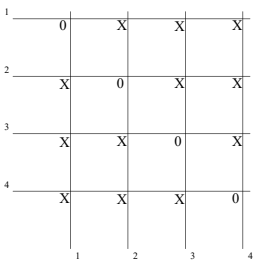

Fig. 1: *Diagonal-0* coded 4×4 array

III. Probabilities and Joint Probabilities of Sneak Path Event

In the previous section, we proposed the *diagonal-0* coding construction for the resistive memory array. In order to utilize the known 0s on the diagonal for more informed estimation schemes, several important probabilities need to be calculated analytically. In this section, we first point out the important probabilities that will be used in the following section; we then focus on the calculation of those probabilities. First, in order to determine the sneak-path state of a precoded diagonal bit, we need $P(e_{ii})$. Second, in order to use the sneak-path state at diagonal cells for more informed estimation schemes, we need $P(e_{ij}|e_{ii}, A_{ij} = 0) = P(e_{ij}|e_{jj}, A_{ij} = 0)$ and $P(e_{ij}|e_{ii}, e_{jj}, A_{ij} = 0)$ for $i \neq j$. The two sets of conditional probabilities are used in different estimation schemes in the following section. To make a comparison with the scheme that does not use any side information, we also need $P(e_{ij}|A_{ij} = 0)$. Note that all probabilities calculated in this section are conditioned on the fact that the array is *diagonal-0* coded (we omit this condition for clarity). We assume that the information bits are chosen i.i.d. Bernoulli with parameter q representing the prior probability of a 1 being stored. We start with the calculation of $P(e_{ii})$ by calculating $P(e_{ii} = 0)$. For the rest of this work, we use the two indexes, i and j, where $i \neq j$.

Lemma 1. *In an $n \times n$ diagonal-0 coded array, the probability that no sneak-path event occurs at cell (i, i) is*

$$P(e_{ii} = 0) = \sum_{u=0}^{n-1} \sum_{v=0}^{n-1} \sum_{k=\max(0,u+v-n+1)}^{\min(u,v)} \left[\binom{n-1}{u} \binom{u}{k} \binom{n-1-u}{v-k} q^{u+v} (1-q)^{n-1-u+n-1-v} (1-p_f q)^{uv-k} \right]. \quad (3)$$

Proof. We derive this probability by conditioning on the number of 1s in the i-th row (v), the number of 1s in the i-th column (u), and the number of overlapping indexes between the columns that contain the v ones and the rows that contain the u ones (k). For certain u, v, and k, there is no sneak-path event affecting cell (i, i) if each of the cells on the intersection

of the v columns and u rows, excluding the precoded k cells, either contains 0 or contains 1 and the selector does not fail. Summing the probabilities of bit assignments gives (3). ■

Next we calculate $P(e_{ij}|A_{ij}=0)$ by calculating $P(e_{ij}=0|A_{ij}=0)$.

Lemma 2. *In an $n\times n$ diagonal-0 coded array, the probability that no sneak-path event occurs at cell (i,j), given a 0 stored at cell (i,j), is*

$$P(e_{ij}=0|A_{ij}=0)=\sum_{u=0}^{n-2}\sum_{v=0}^{n-2}\sum_{k=\max(0,u+v-n+2)}^{\min(u,v)}\left[\binom{n-2}{u}\binom{u}{k}\binom{n-2-u}{v-k}q^{u+v}(1-q)^{n-2-u+n-2-v}(1-p_fq)^{uv-k}\right]. \tag{4}$$

Next we compute $P(e_{ij}|e_{jj},A_{ij}=0)$ by first computing $P(e_{ij}=0,e_{jj}=0|A_{ij}=0)$.

Lemma 3. *In an $n\times n$ diagonal-0 coded array, the joint probability that no sneak-path events occur at cell (i,j) and cell (j,j), given a 0 stored at cell (i,j), can be calculated with Equation (5), as shown at bottom of the page, where*

$$P^{(3)}_{u,v,u',o,k}=\binom{n-2}{u}\binom{u}{o}\binom{n-2-u}{u'-o}\binom{u+u'-o}{k}\binom{n-2-u-u'+o}{v-k}q^{u+u'+v}(1-q)^{n-2-u+n-2-u'+n-2-v}, \tag{6}$$

and

$$P^{(3)}_{e0|u,v,u',o,k}=(1-p_fq)^{v(u+u'-o)-k}. \tag{7}$$

Proof. The proof proceeds by summing up the probabilities of two cases, $A_{ji}=0$ and $A_{ji}=1$. When $A_{ji}=0$, we condition on the number of 1s on the i-th row (v), the number of 1s on the j-th column (u), the number of 1s on the i-th column (u'), the number of overlapping indexes between the u rows and u' rows (o), and the number of overlapping indexes between the $u+u'-o$ rows and the v columns (k). When $A_{ji}=1$, we use the same conditions and have $u+u'-o+1$ rows that have 1s at either the i-th column or the j-th column. The rest of the proof is similar to the proof of Lemma 1. ■

Using (5) together with the marginal probabilities $P(e_{ij}|A_{ij}=0)$ and $P(e_{jj}|A_{ij}=0)$ (computable using the next corollary), we can compute all $P(e_{ij}|e_{jj},A_{ij}=0)$.

Corollary 3.1.

$$P(e_{jj}=0|A_{ij}=0)=\sum_{u=0}^{n-1}\sum_{v=0}^{n-2}\sum_{k=\max(0,u+v-n+1)}^{\min(u,v)}\left[\binom{n-2}{v}\binom{v}{k}\binom{n-1-v}{u-k}q^{u+v}(1-q)^{n-1-u+n-2-v}(1-p_fq)^{uv-k}\right]. \tag{8}$$

Finally we calculate $P(e_{ij}|e_{ii},e_{jj},A_{ij}=0)$ by first calculating $P(e_{ij}=0,e_{ii}=0,e_{jj}=0|A_{ij}=0)$.

Lemma 4. *In an $n\times n$ diagonal-0 coded array, the joint probability that no sneak-path events occur at cell (i,j), cell (j,j), and cell (i,i), given a 0 stored at cell (i,j), is*

$$P(e_{ij}=0,e_{ii}=0,e_{jj}=0|A_{ij}=0)=\sum_{u=0}^{n-2}\sum_{u'=0}^{n-2}\sum_{o=\max(0,\,u+u'-n+2)}^{\min(u,u')}\sum_{k=0}^{u}\sum_{k^*=0}^{u'-o}\sum_{w=0}^{n-2-u-u'+o}\sum_{v=0}^{k+k^*+w}\sum_{v^*=\max(0,\,v-k-w)}^{\min(v,k^*)}\sum_{v'=k+k^*+w-v}^{k+k^*+w}\left[\binom{n-1}{u}\binom{u}{o}\binom{n-2-u}{u'-o}\binom{u'-o}{k^*}\binom{n-2-u-u'+o}{w}\binom{k^*}{v^*}\binom{k+w}{v-v^*}\binom{v}{v-k-k^*-w+v'}q^{u+u'+v+v'}(1-q)^{2n-4-u-u'}(1-q)^{2n-4-v-v'}(1-p_fq)^{uv+uv'+vu'-ov-u(v-k-k^*-w+v)-k-v^*}\times\left[(1-q)+q(1-p_f)^{o+v-k-k^*-w+v'}\right]\right]. \tag{9}$$

Proof. The proof proceeds by summing up the probabilities of two cases, $A_{ji}=0$ and $A_{ji}=1$. When $A_{ji}=0$, we condition on the number of 1s on the i-th row (v), the number of 1s on the j-th row (v'), the number of 1s on the j-th column (u), the number of 1s on the i-th column (u'), the number of overlapping indexes between the u rows and u' rows (o), the number of overlapping indexes between the u rows and the columns that contain the union of v ones and v' ones (k), the number of overlapping indexes between the $u'-o$ rows and the columns that contain the union of v ones and v' ones (k^*), the number of indexes of the columns that contain the union of v ones and v' ones that differ from the indexes of the $u+u'-o$ rows (w) and the number of overlapping indexes between the k^* columns and the v columns (v^*). Under each condition, there are $uv+uv'+vu'-ov-u(v-k-k^*-w+v)-k-v^*$ cells that have to either store 0 or store 1 with a non-failing cell selector by the geometry of this problem. When $A_{ji}=1$, we additionally require the cells on the i-th column that store the overlapping 1s between the u and u' 1s to not fail

$$P(e_{ij}=0,e_{jj}=0|A_{ij}=0)=\sum_{v=0}^{n-2}\sum_{u=0}^{n-2}\sum_{u'=0}^{n-2}\sum_{o=\max(0,\,u+u'-n+2)}^{\min(u,u')}\sum_{k=\max(0,u+u'-o+v-n+2)}^{\min(u+u'-o,v)}\left[P^{(3)}_{u,v,u',o,k}\left[(1-q)P^{(3)}_{e0|u,v,u',o,k}+qP^{(3)}_{e0|u,v,u',o,k}(1-p_fq)^v\right]\right] \tag{5}$$

simultaneously, as well as the cells on the j-th row that store the overlapping 1s between the v and v' 1s. The rest of the proof is similar to the proof of Lemma 1. ■

Using the above probability together with the probabilities $P(e_{ij}, e_{ii}|A_{ij} = 0) = P(e_{ij}, e_{jj}|A_{ij} = 0)$ and $P(e_{ii}, e_{jj}|A_{ij} = 0)$, we compute all probabilities of the form $P(e_{ij}|e_{ii}, e_{jj}, A_{ij} = 0)$. The probabilities $P(e_{ii}, e_{jj}|A_{ij} = 0)$ can be approximated by assuming that the sneak-path events on diagonal cells occur independently.

IV. Adaptive Thresholding Schemes

With all conditional probabilities calculated, we propose our adaptive thresholding schemes. We propose two schemes, the *Double Threshold Scheme* based on single precoded 0 on the diagonal and the *Triple Threshold Scheme* based on two precoded 0s. We also state the *Single Threshold Scheme* which uses no side information for comparison. For the two adaptive thresholding schemes, first we determine the sneak-path states of the precoded 0s on the diagonal, then based on these sneak-path states of the 0s, we choose appropriate thresholds to decide the states of the cells to be read. All decisions are made through a sub-optimal threshold estimators for implementation simplicity. We deduce the optimal thresholds for the threshold estimators in the next sections. In following subsections, the probability density function of the Gaussian addictive noise η in Equation (2) is defined to be $f_\eta(\cdot)$.

A. Optimal Threshold Estimation for Precoded Cells

We define τ_s to be the threshold for the estimation of a sneak-path event on the precoded diagonal cells. For the precoded 0s on the diagonal, we have two hypotheses, $e_{ii} = 0$ and $e_{ii} = 1$. Based on our modeling in Equation (2), the posterior function of each hypothesis can be expressed as

$$\Lambda_{e_{ii}}(r_{ii}) = f_\eta\left(r_{ii} - \left(\frac{1}{R_0} + \frac{e_{ii}}{R_s}\right)^{-1}\right) P(e_{ii}). \quad (10)$$

For a given resistance measurement r_{ii}, the output of this threshold estimator is

$$\hat{e}_{ii} = \begin{cases} 1 & \text{if} \quad 0 \le r_{ii} \le \tau_s, \\ 0 & \text{if} \quad \tau_s \le r_{ii} \le \infty. \end{cases} \quad (11)$$

Minimizing the error probability of this threshold estimator by Bayes Criterion gives the condition:

$$\Lambda_{e_{ii}=1}(\tau_s) = \Lambda_{e_{ii}=0}(\tau_s). \quad (12)$$

Solving (12) gives the following optimal τ_s:

$$\tau_s = \frac{1}{2}\frac{R_0^2 - \left(\frac{1}{R_0} + \frac{1}{R_s}\right)^{-2} + 2\sigma^2 \log\left(\frac{P(e_{ii}=1)}{P(e_{ii}=0)}\right)}{R_0 - \left(\frac{1}{R_0} + \frac{1}{R_s}\right)^{-1}}. \quad (13)$$

B. Optimal Threshold Estimation for Read Cells

In this subsection, we calculate the optimal thresholds for the three thresholding schemes, assuming the sneak-path states of the precoded cells are known. The three thresholding schemes are alike and only differ on the side-information used for each scheme. Therefore, we use the variable c to denote the side-information used in each scheme to describe the three schemes collectively. We let $c = \{\}$ for the *Single Threshold Scheme*, $c = \{e_{jj}\}$ for the *Double Threshold Scheme*, and $c = \{e_{ii}, e_{jj}\}$ for the *Triple Threshold Scheme*.

For the read cell (i, j), we have two hypotheses, $A_{ij} = 0$ and $A_{ij} = 1$. Based on different thresholding schemes and the actual value of c, the posterior functions of each hypothesis given r_{ij} are

$$\Lambda_{A_{ij}=0}(r_{ij}) = (1-q)\Bigg[f_\eta(r_{ij} - R_0)P(e_{ij} = 0|A_{ij} = 0, c) + f_\eta\left(r_{ij} - \left(\frac{1}{R_0} + \frac{1}{R_s}\right)^{-1}\right) P(e_{ij} = 1|A_{ij} = 0, c)\Bigg], \quad (14)$$

and

$$\Lambda_{A_{ij}=1}(r_{ij}) = q f_\eta(r_{ij} - R_1). \quad (15)$$

We define τ_{naive} to be the threshold used in the *Single Threshold Scheme*; τ_0 and τ_1 to be the thresholds used in the *Double Threshold Scheme*; τ_{00}, τ_{01}, and τ_{11} to be the thresholds used in the *Triple Threshold Scheme*. We match τ_{naive},τ_0,τ_1,τ_{00}, and τ_{11} with the conditions $c = \{\}, \{e_{jj} = 0\}, \{e_{jj} = 1\}, \{e_{ii} = 0, e_{jj} = 0\}$, and$\{e_{ii} = 1, e_{jj} = 1\}$, respectively. The threshold τ_{01} is used for the conditions $c = \{e_{ii} = 0, e_{jj} = 1\}$and $c = \{e_{ii} = 1, e_{jj} = 0\}$ due to symmetry. Denoting these thresholds collectively by τ_c, for each thresholding schemes and corresponding conditions, when reading cell (i, j), the output of that threshold estimator is

$$\hat{A}_{ii} = \begin{cases} 1 & \text{if} \quad 0 \le r_{ij} \le \tau_c, \\ 0 & \text{if} \quad \tau_c \le r_{ij} \le \infty. \end{cases} \quad (16)$$

Minimizing the error probability of this threshold estimator by Bayes Criterion gives the condition:

$$\Lambda_{A_{ij}=1}(\tau_c) = \Lambda_{A_{ij}=0}(\tau_c). \quad (17)$$

Although numerical solution of (17) can be found, similar to [11], we give an approximate solution to highlight the dependency on parameters. This approximation follows by approximating the two Gaussian functions in (14) with a single Gaussian function that is closest to the Gaussian function in (15). This approximation captures the locally behavior of (14) near the threshold as the two Gaussian functions are sufficiently apart. The threshold values with this approximation are

$$\tau_c \approx \frac{1}{2}\frac{\left(\frac{1}{R_0} + \frac{1}{R_s}\right)^{-2} - R_1^2 + 2\sigma^2 \log\left(\frac{q}{(1-q)P(e_{ii}=1|A_{ij}=0,c)}\right)}{\left(\frac{1}{R_0} + \frac{1}{R_s}\right)^{-1} - R_1}. \quad (18)$$

These thresholds can be precomputed and stored in a table if the *Double Threshold Scheme* is used.

Note that although Gaussian measurement noise is used for mathematical simplicity, other models of the measurement noise, such as log-normal distribution [13], can be easily adopted with only changes in the thresholds calculations.

Figure 2 provides an example of the posterior distribution of the two hypotheses given the following conditions: no side information, $e_{jj} = 0$, and $e_{jj} = 1$. It is clear that changing the

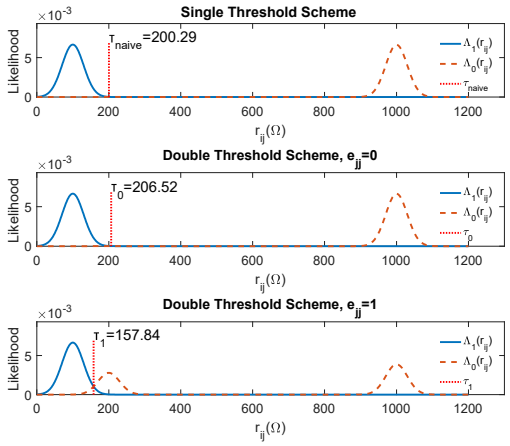

Fig. 2: Example of posterior distributions and the optimal thresholds: $R_1 = 100\Omega$, $R_0 = 1000\Omega$, $R_s = 250\Omega$, $p_f = 10^{-3}$, and $\sigma = 30$.

threshold adaptively decreases the probability of estimation error. In the example, when $e_{jj} = 1$, the error probability is higher if τ_{naive} is used as the threshold.

C. Estimation Procedures

For the *Double Threshold Scheme* and the *Triple Threshold Scheme*, the following procedure is performed every time a page of resistive memory is written:

- Measure the resistances of cells on the diagonal and determine $\hat{e}_{ii}, i \in [1, \cdots, n]$ using τ_s.

This step can be thought of as a form of channel estimation and is not necessary for the *Single Threshold Scheme.* The following is then performed:

- If the *Double Threshold Scheme* is used, since every cells on the same row(column) will be using the same threshold value, the threshold values τ_0 and τ_1 can be hardware configured for each row(column) based on $\hat{e}_{ii}(\hat{e}_{jj})$.
- If the *Triple Threshold Scheme* is used, the sneak-path state is stored for future use.

When reading cell (i, j), the estimator does the following:

- If the *Single Threshold Scheme* is used, measure r_{ij} and use τ_{naive} to decide $\hat{A}_{ij}$.
- If the *Double Threshold Scheme* is used, measure r_{ij} and use the pre-configured threshold to decide $\hat{A}_{ij}$.
- If the *Triple Threshold Scheme* is used, measure r_{ij}, look for $\hat{e}_{ii}$ and $\hat{e}_{jj}$ in a table, and use the appropriate threshold to decide $\hat{A}_{ij}$.

V. Simulation Results

In this section, the two adaptive thresholding schemes proposed in this paper are evaluated via simulation and are compared with the *Single Threshold Scheme*. Bit-error rate (BER) is used as our performance metric for these schemes. In the simulations, we use prior probability $q = 0.5$ and the following resistance values: $R_1 = 100\Omega$, $R_0 = 1000\Omega$, and $R_s = 250\Omega$, (same as [11]). In different simulations, we vary the parameters σ, n and p_f to test their influence on the performance of our schemes.

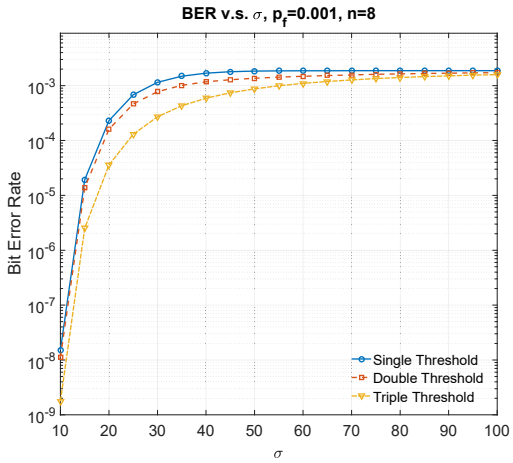

Fig. 3: BER of thresholding schemes at various noise levels

First, we fix $p_f = 10^{-3}$ and $n = 8$ to study the influence of noise on the thresholding schemes. Figure 3 shows that both *Double Threshold Scheme* and *Triple Threshold Scheme* show notable improvements on BER in a noise regime of $20\% - 50\%$ of R_1. The two schemes both saturate together with the *Single Threshold Scheme* at high noise level. This can be explained by observing that when two Gaussian already overlap by a lot, moving the threshold have no significant effect on the error probability. At low noise regime, while the *Double Threshold Scheme* shows similar performance with the *Single Threshold Scheme*, the *Triple Threshold Scheme* still shows an order of magnitude improvement, thus a single precoded 0 does not provide enough information to move the threshold at low noise levels compared with two precoded 0s.

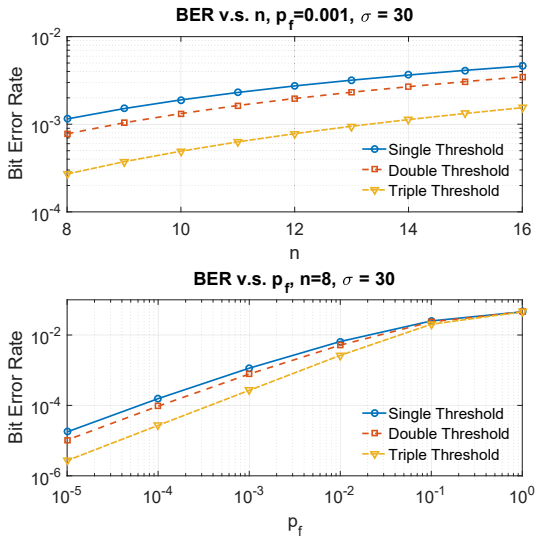

Fig. 4: BER of thresholding schemes under various p_f and n

We then compare the thresholding schemes under various p_f and n; the results are shown in Figure 4. As the array scales, the improvement of using the adaptive thresholding schemes decreases, e.g., comparing the *Single Threshold Scheme* and *Triple Threshold Scheme*, the improvement comes

from a factor of 4.26 ($n = 8$) down to a factor of 2.99 ($n = 16$). As the cell selectors are more prone to failure, the improvement of using the adaptive thresholding schemes also decreases. These two observations are explained as follows: increasing either n or p_f increases the probability of a sneak-path event. An increased probability of a sneak-path event results in optimal thresholds under different conditions that are close to each other. Thus, small changes in the threshold values cause the improvement from adaptive thresholding schemes to be insignificant.

VI. Conclusion

In this paper, utilizing the inter-cell dependency of sneak-path events, we provide a light-weight estimation theoretic scheme to mitigate the sneak-path problem in resistive memory. This work can be extended in many directions. For future theoretical developments, a theoretical analysis of BER performance can be developed. These adaptive thresholding techniques can be combined with constraint coding solutions to alleviate sneak-path problem in arrays without cell selectors. SPICE simulation with real memristor model can be also done to test our adaptive thresholding schemes.

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