Hardware Implementation Analysis of Non-Binary LDPC Decoders

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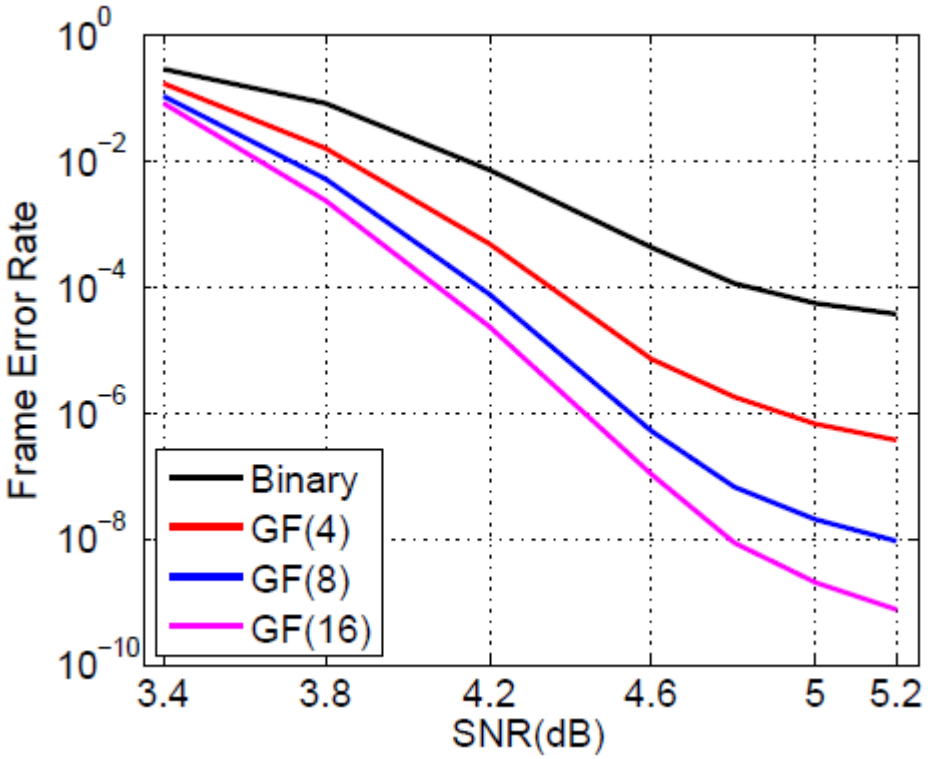
Non-Binary LDPC Decoding

- **High-performance error correction with low error floor**
  - Improved performance over their binary counterparts
  - Increasing GF(q) improves frame error rate (FER) at a significant hardware cost



Bit length: 2209, Rate: 0.91

Column weight: 4

Row weight: 47

Challenges in Hardware Implementation

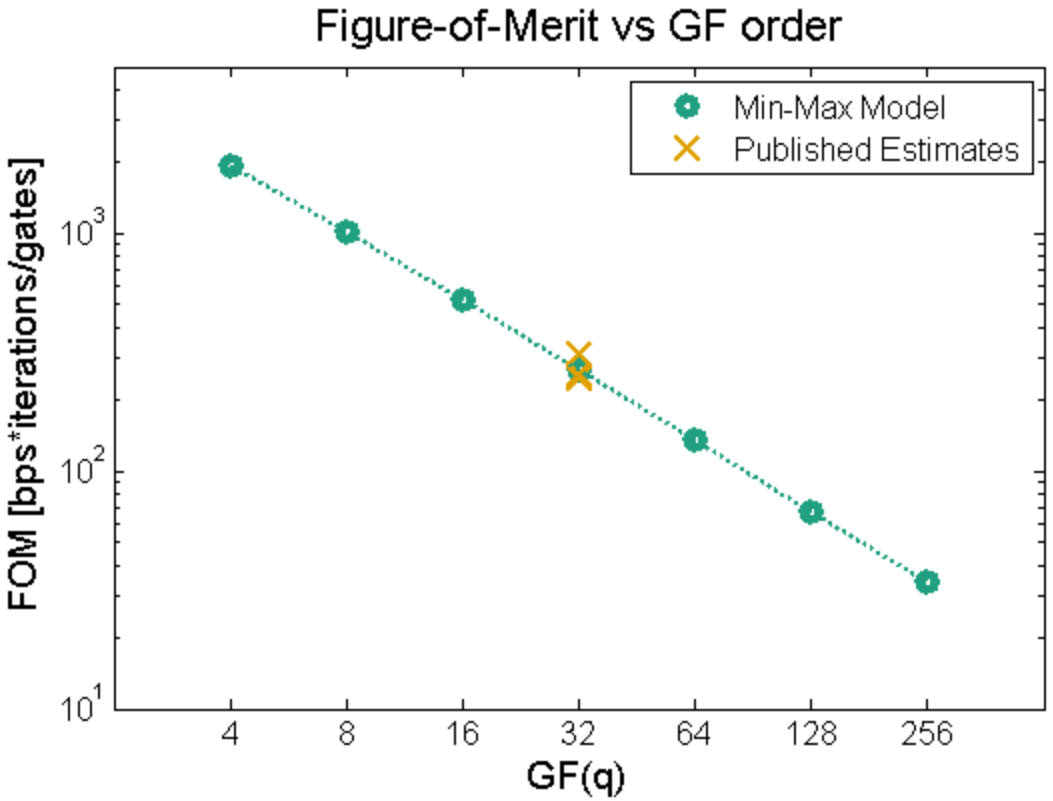
- **Decoder occupies large area even for low throughputs**
- **Hardware complexity scaling with field order is unquantified**

	[1]			[2]			[3]
GF(q)	32	32	32	32	32	32	32
Symbol Length	620	744	837	837	620	248	837
(dv, dc)	(3, 6)	(3, 24)	(4, 27)	(4, 27)	(3, 6)	(4, 8)	(4, 27)
Throughput (Mbps)	21	21	16	29	66.6	47.7	10
Gate count (NAND)	1.24M	1.07M	1.37M	3.28M	2.14M	1.92M	1.6M

[1] *Chen, X., et. al., "Efficient Configurable Decoder Architecture for Nonbinary Quasi-Cyclic LDPC Codes," T-CAS I, Jan. 2012.*
[2] *Ueng, Y.-L., et. al., "An Efficient Layered Decoding Architecture for Nonbinary QC-LDPC Codes," T-CAS I, Feb. 2012.*
[3] *Zhang, X., Cai, F., "Reduced-Complexity Decoder Architecture for Non-Binary LDPC Codes," T-VLSI, July 2011.*

Proposed Resource Model

- **Resource estimation model developed to estimate hardware cost tradeoff for GF(q)**
- **Compared against published works (estimated FOM) for accuracy**

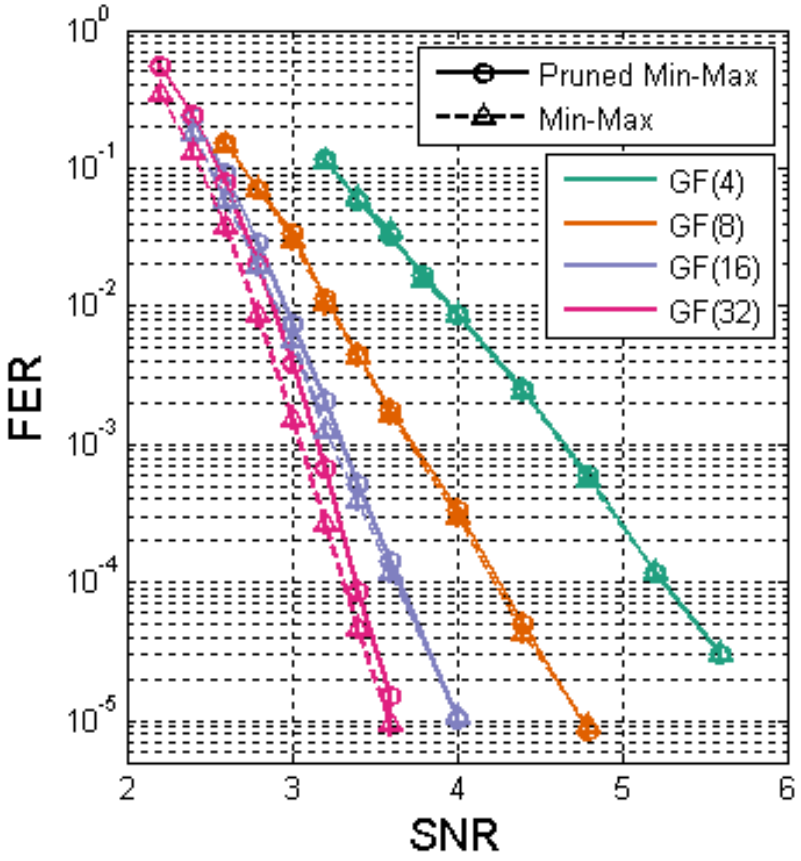


Allows exploration of the decoder-design space

[1] *Chen, X., et. al., "Efficient Configurable Decoder Architecture for Nonbinary Quasi-Cyclic LDPC Codes," T-CAS I, Jan. 2012.*
[2] *Ueng, Y.-L., et. al., "An Efficient Layered Decoding Architecture for Nonbinary QC-LDPC Codes," T-CAS I, Feb. 2012.*

Pruned Min-Max: A Simplified Decoding Algorithm

- **Check node computations dominate decoding complexity**
- **Prune the search space for GF(q) elements that satisfy the check equation**
- **Negligible performance degradation compared to the original Min-Max Algorithm**



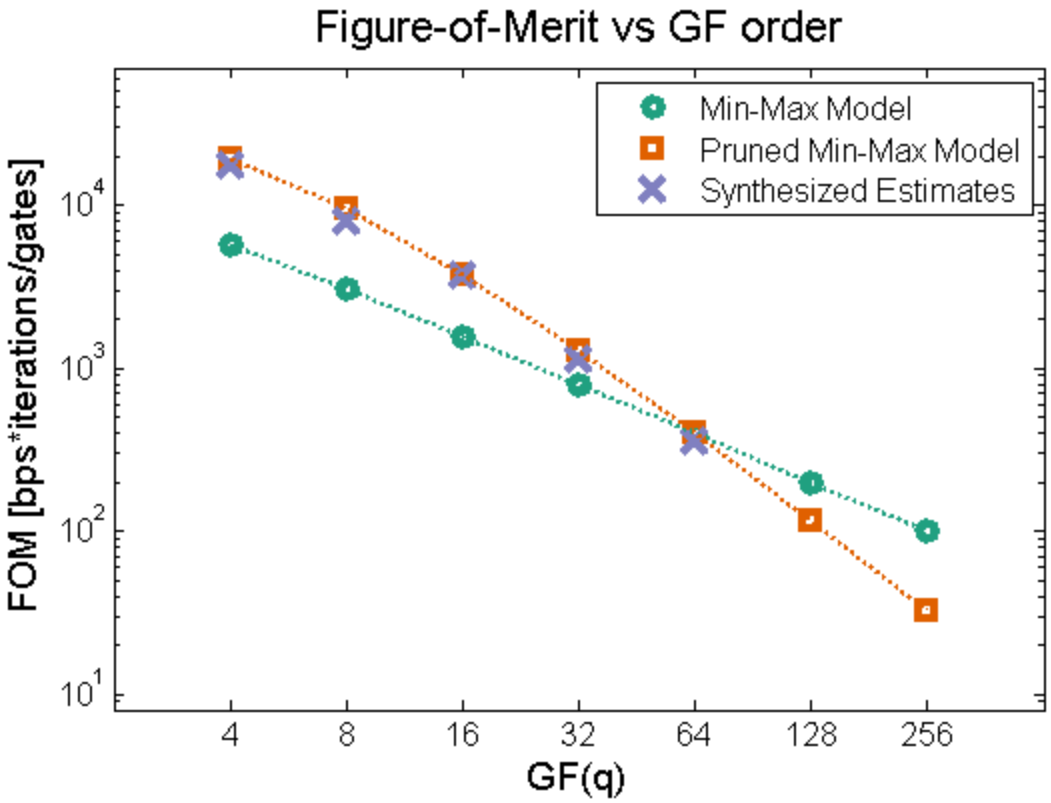
Bit length: ~1500, Rate: 0.5

Column weight: 3

Row weight: 6

Hardware Resource Estimation

- **Resource model quantifies the benefits of the proposed algorithm**
- **Estimates from the model match synthesis estimates**



Up to ~3.4x higher FOM with Pruned Min-Max (GF(4))

Future Work and Goals

- Expand model to incorporate power estimations
- Investigate further algorithmic improvements
- Pursue corresponding intelligent digital design implementations
- Establish feasibility of NB-LDPC decoders as a replacement candidate for binary LDPC decoders